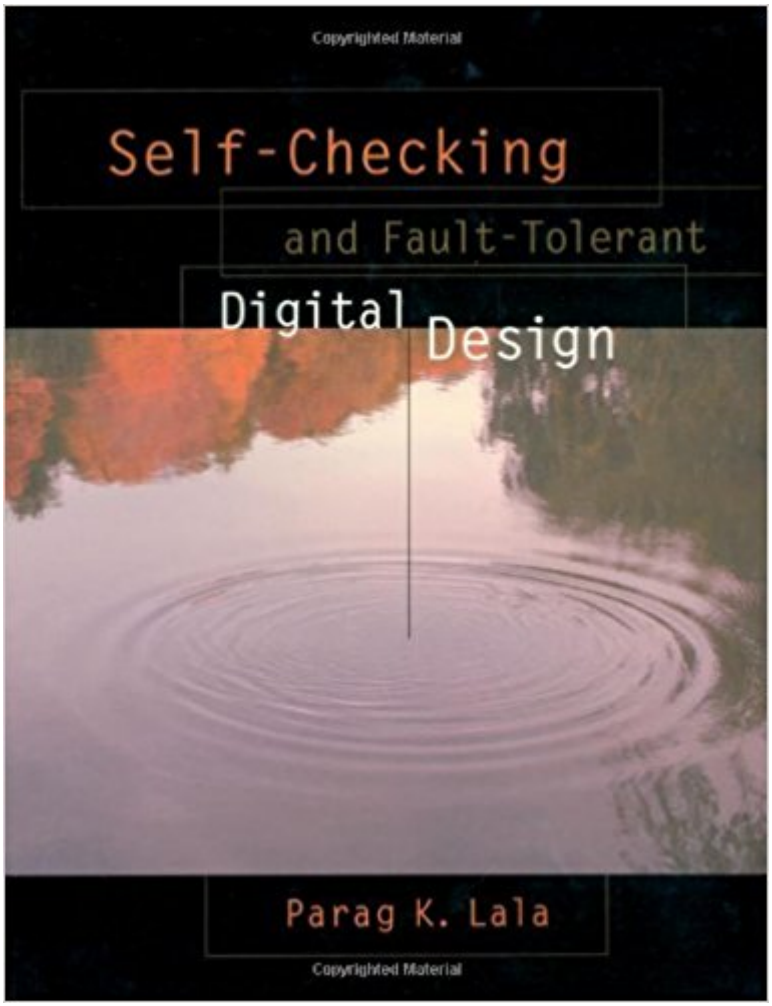
Self-Checking And Fault-Tolerant Digital Design (The Morgan Kaufmann Series In Computer Architecture And Design)



Synopsis

With VLSI chip transistors getting smaller and smaller, today's digital systems are more complex than ever before. This increased complexity leads to more cross-talk, noise, and other sources of transient errors during normal operation. Traditional off-line testing strategies cannot guarantee detection of these transient faults. And with critical applications relying on faster, more powerful chips, fault-tolerant, self-checking mechanisms must be built in to assure reliable operation.Self-Checking and Fault-Tolerant Digital Design deals extensively with self-checking design techniques and is the only book that emphasizes major techniques for hardware fault tolerance. Graduate students in VLSI design courses as well as practicing designers will appreciate this balanced treatment of the concepts and theory underlying fault tolerance along with the practical techniques used to create fault-tolerant systems. * Introduces reliability theory and the importance of maintainability* Presents coding and the construction of several error detecting and correcting codes* Discusses in depth, the available techniques for fail-safe design of combinational circuits* Details checker design techniques for detecting erroneous bits and encoding output of self-checking circuits* Demonstrates how to design self-checking sequential circuits, including a technique for fail-safe state machine design

Book Information

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Customer Reviews

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The author is currently a Professor in the Department of Electrical Engineering at North Carolina A&T State University. He is the author of more than 75 papers, and three books published by Prentice Hall. His research interests include design for testability, self-checking logic design, automatic logic synthesis of low power logic circuits, andCPLD/FPGA based system design. He received a M.S. from King's College, London, and a Ph.D. from the City University of London.

I liked this book as a way to understand the need and use of fault-tolerant logic design. What it lacked is how one would do it using an HDL. Knowing 'what' is generally most useful when how is presented as well. I didn't want to design to the gate level to gain the benefit of these principals. So, after I read it I was left hungry for a solution.

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